

## CLAIMS

What is claimed is:

- 1           1.     A mixed signal circuit comprising:  
2                 a plurality of fixed threshold and variable threshold transistors;  
3                 a plurality of Schottky barrier diodes;  
4                 a plurality of poly silicon film resistors;  
5                 a plurality of capacitors; and  
6                 a plurality of wiring tracks, wherein all of the elements are on a single  
7     substrate to form integrated circuits with implementing macro functions.
- 1           2.     The mixed signal circuit of claim 1 wherein the circuit is software driven.
- 1           3.     The mixed signal circuit of claim 2 wherein software is provided to adjust the  
2     threshold of the variable threshold transistors.
- 1           4.     The mixed signal circuit of claim 2 wherein software is provided to form  
2     reconfigurable logic gate array circuit units.
- 1           5.     The mixed signal circuit of claim 2 wherein software is provided to complete  
2     certain network connections among various units in the single diagram.

1           6.     The mixed signal circuit of claim 2 wherein the software includes state  
2 tables, virtual machines, setup or initialization and test procedures, data access, transport,  
3 and storage algorithms.

1           7.     The mixed signal circuit of claim 1 wherein the circuit is hardware driven,  
2 wherein the hardware comprises hardwired Schottky CMOS Logic (SCL) gate array and  
3 memory units, IO transceivers, and terminators.

1           8.     The mixed signal circuit of claim 7 wherein the hardware comprises software  
2 driven SCL gate arrays, IO transceivers, terminators, capacitors and wherein a switch  
3 transistor is of VT type.

1           9.     The mixed signal circuit of claim 7 which includes software driven SCL gate  
2 arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT type,  
3 and the SCL unit act as analog signal comparator.

1           10.    The mixed signal circuit of claim 7 which includes software driven SCL gate  
2 arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT type,  
3 and the SCL gate may perform a nonvolatile latch function.

1           11.    The mixed signal circuit of claim 7 which includes software driven SCL gate  
2 arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT type,

3 and the SCL unit may process multi-value logic operation with binary, ternary and  
4 quaternary operators.

1 12. The mixed signal circuit of claim 7 which includes software driven CMOS-  
2 TTL gate arrays, IO transceivers, terminators and capacitors.

1 13. The mixed signal circuit of claim 7 which includes hardwired conventional  
2 logic and memory units including but not limited to CMOS-TTL gate arrays, Register files,  
3 embedded RAM, ROM and Flash cores.

1 14. The mixed signal circuit of claim 7 which includes dedicated programming  
2 facilities of voltage and current sources, clock and oscillators, state machines and counters,  
3 to implement and control both cell wise and block wise cell operations and which is shared  
4 to alter the charge storage or VT threshold of the selected device(s) in the logic and (Flash)  
5 memory circuitry.

1 15. The mixed signal circuit of claim 1 wherein the SBDs comprise a PN  
2 junction diode if SOI GaAs technologies are used.

1 16. The mixed signal circuit of claim 1 wherein the SBD can be coupled to input  
2 pads for Electrical Static Discharge protection.

1           17.     The mixed signal circuit of claim 1 wherein the SBD can be coupled to the  
2 well for Latch-up suppression.

1           18.     The mixed signal circuit of claim 1 wherein the SBD can be coupled to  
2 control the well biasing potential, therefore change I-V characteristics of CFETs within the  
3 well region with circuit operating conditions.

1           19.     The mixed signal circuit of claim 3 wherein the SBDs are adaptable to other  
2 product applications including but not limited to DRAM, Flash, CAM, PLD, ROM, and  
3 embedded ASICs.

1           20.     A mixed signal circuit comprising:  
2 a plurality of fixed threshold and variable threshold transistors;  
3 a plurality of Schottky barrier diodes;  
4 a plurality of poly silicon film resistors;  
5 a plurality of capacitors; and  
6 a plurality of wiring tracks, wherein all of the elements are on a single substrate to  
7 form integrated circuits with implementing macro functions, wherein the circuit is software  
8 driven and wherein the at least a portion of the macro functions can be hardwired  
9 macroassets.

1           21.     The mixed signal circuit of claim 20 wherein software is provided to adjust  
2 the threshold of the variable threshold transistors.

1           22.     The mixed signal circuit of claim 20 wherein software is provided to form  
2     reconfigurable logic gate array circuit units.

1           23.     The mixed signal circuit of claim 20 wherein software is provided to  
2     complete certain network connections among various units in the single diagram.

1           24.     The mixed signal circuit of claim 20 wherein the software includes state  
2     tables, virtual machines, setup or initialization and test procedures, data access, transport  
3     and storage algorithms.

1           25.     The mixed signal circuit of claim 20 wherein the circuit is hardware driven,  
2     wherein the hardware comprises hardwired Schottky CMOS Logic (SCL) gate array and  
3     memory units, IO transceivers, and terminators.

1           26.     The mixed signal circuit of claim 25 wherein the hardware comprises  
2     software driven SCL gate arrays, IO transceivers, terminators, capacitors and wherein a  
3     switch transistor is of VT type.

1           27.     The mixed signal circuit of claim 25 which includes software driven SCL  
2     gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT  
3     type, and the SCL unit act as analog signal comparator.

1           28.     The mixed signal circuit of claim 25, which includes software driven SCL  
2 gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT  
3 type, and the SCL gate may perform a nonvolatile latch function.

1           29.     The mixed signal circuit of claim 25 which includes software driven SCL  
2 gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT  
3 type, and the SCL unit may process multi-value logic operation with binary, ternary and  
4 quaternary operators.

1           30.     The mixed signal circuit of claim 25 which includes software driven CMOS-  
2 TTL gate arrays, IO transceivers, terminators and capacitors.

1           31.     The mixed signal circuit of claim 25 which includes hardwired conventional  
2 logic and memory units including but not limited to CMOS-TTL gate arrays, Register files,  
3 embedded RAM, ROM and Flash cores.

1           32.     The mixed signal circuit of claim 25 which includes dedicated programming  
2 facilities of voltage and current sources, clock and oscillators, state machines and counters,  
3 to implement and control both cell wise and block wise cell operations and which is shared  
4 to alter the charge storage or VT threshold of the selected device(s) in the logic and (Flash)  
5 memory circuitry.

1           33.     A mixed signal circuit comprising:

2 a plurality of fixed threshold and variable threshold transistors;  
3 a plurality of Schottky barrier diodes;  
4 a plurality of poly silicon film resistors;  
5 a plurality of capacitors; and  
6 a plurality of wiring tracks, wherein all the elements are on a single substrate  
7 to form integrated circuits with implementing macro functions, wherein a part of the  
8 elements are user programmed and part of the elements are factory programmable, wherein  
9 the circuit is software driven.

1 34. The mixed signal circuit of claim 33 wherein software is provided to adjust  
2 the threshold of the variable threshold transistors.

1 35. The mixed signal circuit of claim 33 wherein software is provided to form  
2 reconfigurable logic gate array circuit units.

1 36. The mixed signal circuit of claim 33 wherein software is provided to  
2 complete certain network connections among various units in the single diagram.

1 37. The mixed signal circuit of claim 33 wherein the software includes state  
2 tables, virtual machines, setup or initialization and test procedures, data access, transport,  
3 and storage algorithms.

1           38.     The mixed signal circuit of claim 33 wherein the circuit is hardware driven,  
2           wherein the memory comprises hardwired Schottky CMOS Logic (SCL) gate array and  
3           memory units, IO transceivers, and terminators.

1           39.     The mixed signal circuit of claim 38 wherein the hardware comprises  
2           software driven SCL gate arrays, IO transceivers, terminators, capacitors and wherein a  
3           switch transistor is of VT type.

1           40.     The mixed signal circuit of claim 38 which includes software driven SCL  
2           gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT  
3           type, and the SCL unit act as analog signal comparator.

1           41.     The mixed signal circuit of claim 38 which includes software driven SCL  
2           gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT  
3           type, and the SCL gate may perform a nonvolatile latch function.

1           42.     The mixed signal circuit of claim 38 which includes software driven SCL  
2           gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT  
3           type, and the SCL unit may process multi-value logic operation with binary, ternary and  
4           quaternary operators.

1           43.     The mixed signal circuit of claim 38 which includes software driven CMOS-  
2           TTL gate arrays, IO transceivers, terminators and capacitors.